IN THE CLAIMS:

Claims 1-7. (Canceled)

8. (Currently Amended) An ~~The~~ output buffer circuit ~~according to claim 6, further~~ comprising:

a first drive circuit, connected to an output terminal, for receiving an input signal and generating a first output signal having a first state indicative of one of a high logical level and a low logical level, wherein the first drive circuit includes a first output transistor connected between a first power supply and the output terminal and a second output transistor connected between a second power supply and the output terminal, wherein the first and second output transistors generate the first output signal;

a second drive circuit connected to the output terminal, wherein the second drive circuit generates a second output signal, and wherein the second drive circuit includes a third output transistor connected between the first power supply and the output terminal and a fourth output transistor connected between the second power supply and the output terminal, the third and fourth output transistors having lower impedances than the first and second output transistors;

a first control circuit, connected to the second drive circuit, for generating a first control signal for driving the second drive circuit on the basis of the input signal and a delay signal which is generated by adding a predetermined delay to the first output signal such that the second drive circuit generates the second output signal having the first state; and

a second control circuit, connected to the first drive circuit, for inverting the input signal to generate second and third control signals respectively supplied to the first and second output transistors, wherein the first control circuit generates the first control signal and a fourth control signal that have phases opposite to a phase of the input signal and are respectively supplied to the third and fourth output transistors.

9. (Currently Amended) An ~~The~~ output buffer circuit ~~according to claim 6, further~~ comprising:

a first drive circuit, connected to an output terminal, for receiving an input signal and generating a first output signal having a first state indicative of one of a high logical level and a low logical level, wherein the first drive circuit includes a first output transistor connected between a first power supply and the output terminal and a second output transistor connected between a second power supply and the output terminal, wherein the first and second output transistors generate the first output signal;

a second drive circuit connected to the output terminal, wherein the second drive circuit generates a second output signal, and wherein the second drive circuit includes a third output transistor connected between the first power supply and the output terminal and a fourth output transistor connected between the second power supply and the output terminal, the third and fourth output transistors having lower impedances than the first and second output transistors;

a first control circuit, connected to the second drive circuit, for generating a first control signal for driving the second drive circuit on the basis of the input signal and a delay signal which is generated by adding a predetermined delay to the first output

signal such that the second drive circuit generates the second output signal having the first state; and

a second control circuit, connected to the first drive circuit, for generating second and third control signals respectively supplied to the first and second output transistors, wherein the first control circuit generates the first control signal and a fourth control signal respectively supplied to the third and fourth output transistors.

10. (Currently Amended) An ~~The~~ output buffer circuit ~~according to claim 5,~~ comprising:

a first drive circuit, connected to an output terminal, for receiving an input signal and generating a first output signal having a first state indicative of one of a high logical level and a low logical level;

a second drive circuit connected to the output terminal, wherein the second drive circuit generates a second output signal, wherein the second drive circuit includes a plurality of sub-drive circuits having different impedances, wherein at least one of the sub-drive circuits is selectively enabled to set the output impedance of the second drive circuit; and

a first control circuit, connected to the second drive circuit, for generating a first control signal for driving the second drive circuit on the basis of the input signal and a delay signal which is generated by adding a predetermined delay to the first output signal such that the second drive circuit generates the second output signal having the first state.

11. (Previously Presented) The output buffer circuit according to claim 10, wherein the first control circuit supplies the first control signal to each of the sub-drive circuits based on the input signal and a select signal.

Claims 12-37 (Canceled)